

# Service Repair Documentation

## Level 3 –EL71



Release	Date	Department	Notes to change
R 1.0	23.02.2006	BenQ S CC CES	New document

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## **1 Introduction**

### **1.1 Purpose**

This Service Repair Documentation is intended to carry out repairs on BenQ repair level 3.

### **1.2 Scope**

This document is the reference document for all BenQ authorised Service Partners which are released to repair BenQ Mobile phones up to level 3.

### **1.3 Terms and Abbreviations**

## 2 List of available level 3 parts

(according to Component Matrix V1.16 - check C-market for updates)

Product	ID	Order Number	Description CM
EL71	C1355	L50673-F4475-K1	CAPACITOR 4U7 (Cap-Type13)
EL71	C1356	L50673-F4475-K1	CAPACITOR 4U7 (Cap-Type13)
EL71	D1000	L50610-G6282-D670	IC SGOLD2 PMB8876 X2.1 J11
EL71	D1300	V30145J4683Y 33	IC ASIC D1094ED-MOZART+
EL71	D1360	L50610-B6189-D670	IC LOGIC 2 INPUT NAND NC7SP00L6X
EL71	D1361	L50610-B6186-D670	IC LOGIC 2 INPUT AND NC7SZ08L6X
EL71	D5100	L50610-U6122-D670	IC BLUETOOTH BR6150 PB-FREE
EL71	L1300	L50640-F1100-Y5	COIL HM331(Co-Type6)
EL71	L1301	L50651-F5103-M1	COIL 10U (Co-Type9)
EL71	L1302	L36151-F5103-M7	COIL 10U (Co-Type2)
EL71	N1330	L50620-C6258-D670	IC DC DC BOOST CONVERTER LM2733
EL71	N3500	L506810-C6153-D670	IC ANA RE 2.9V USMD5 PB FREE
EL71	N3800	L36145-K280-Y258	IC FEM HITACHI GSM900 1800 1900 (Fem-Type1)
EL71	N3801		IC MODUL PA QCPM-8861 SMD
EL71	N3911	L50620-L6159-D670	IC TRANCEIVER HD155153NP
EL71	N4800	L506810-C6153-D670	IC ANA RE 2.9V USMD5 PB FREE
EL71	R3967	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
EL71	V1302	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
EL71	V1303	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
EL71	V1305	L50630-C1107-D670	TRANSISTOR SI5933 (Tra-Type2)
EL71	V1400	L50640-D70-D670	DIODE BAV99T (Di-Type9)
EL71	V2100	L50640-D5084-D670	DIODE RB548W (Di-Type8)
EL71	V2302	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
EL71	V2330	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
EL71	V2350	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
EL71	V2404	L36830-C1112-D670	TRANSISTOR SI1902 (Tra-Type4)
EL71	V3961	L36840-D61-D670	DIODE 1SV305 (Di-Type4)
EL71	V3962	L36840-C2074-D670	IC DAC DAC3550A
EL71	V4901	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
EL71	V4903	L50630-C1138-D670	TRANSISTOR FDC633 (Tra-Type12)
EL71	V4904	L50630-C1138-D670	TRANSISTOR FDC633 (Tra-Type12)
EL71	X1510	L50634-Z93-C364	IO-JACK NANO 12-POL
EL71	X1603	L50634-Z97-C458	CONNECTOR SIM CARD READER R65 SHORT
EL71	X2201	L50634-Z97-C461	CONNECTOR BOARD TO BOARD 40-POL 1,5MM
EL71	X2705	L50697-F5008-F306	CONNECTOR BOARD TO BOARD 16-POL
EL71	X3500	L50634-Z97-C460	CONNECTOR BOARD TO BOARD 40-POL 1MM

EL71	X3800	L50634-Z97-C382	CONNECTOR COAX SOCKET SWITCHED 2
EL71	X4899	L50634-Z97-C448	CONNECTOR CARDREADER TRANSFLASH HINGE
EL71	Z1001	L50645-F102-Y22	QUARZ 32,768KHZ (Q-Type3)
EL71	Z1501	L50620-U6067-D670	FILTER EMI (Fi-Type8) PB Free
EL71	Z1601	L50620-U6029-D670	FILTER EMI (Fi-Type6) PB Free
EL71	Z3961	L36145-F260-Y17	QUARZ 26MHZ (Q-Type1)
EL71	Z4801	L50620-U6030-D670	FILTER EMI (Fi-Type9) PB Free
EL71	Z5100	L50645-K280-Y330	FILTER BP BLUETOOTH

### 3 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 ([L36880-N9241-A200](#))
- Adapter cable for Bootadapter due to **new** Lumberg connector ([F30032-P226-A2](#))
- Troubleshooting Frame EL71 ([F30032-P731-A3](#))
- Power Supply
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle ([F30032-P28-A1](#)) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

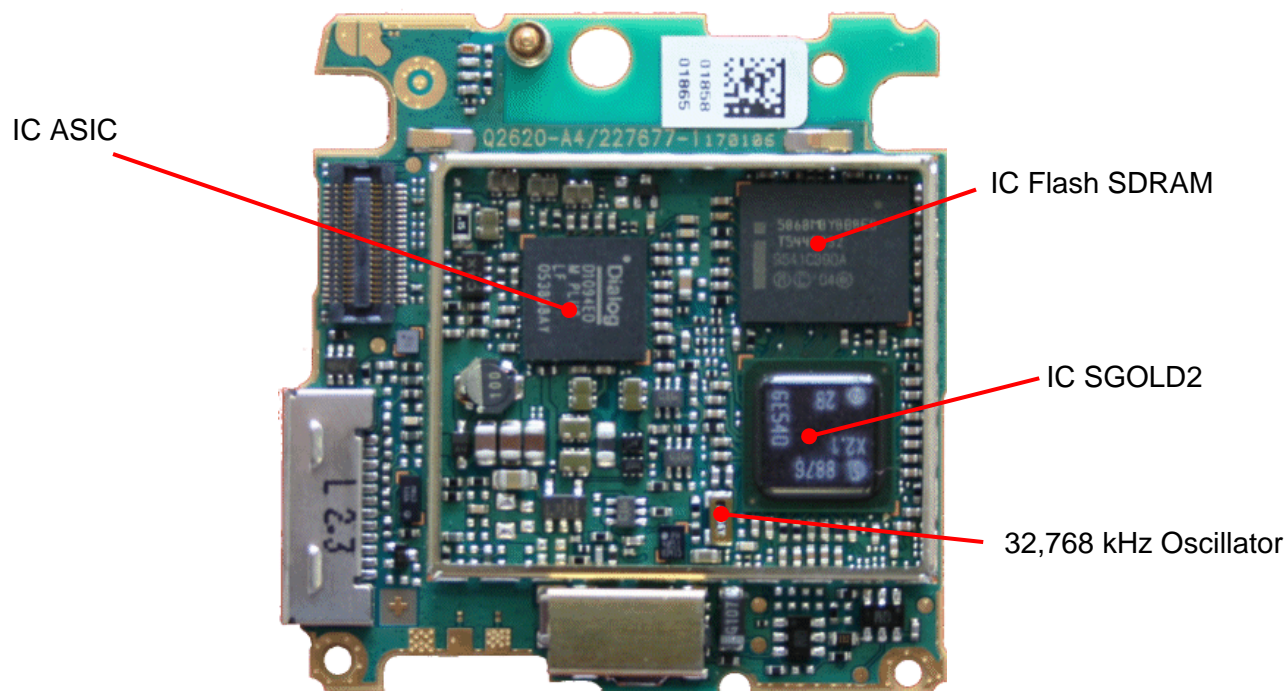
*Reference:* Equipment recommendation V2.0  
(downloadable from the technical support page)

### 4 Required Software for Level 3

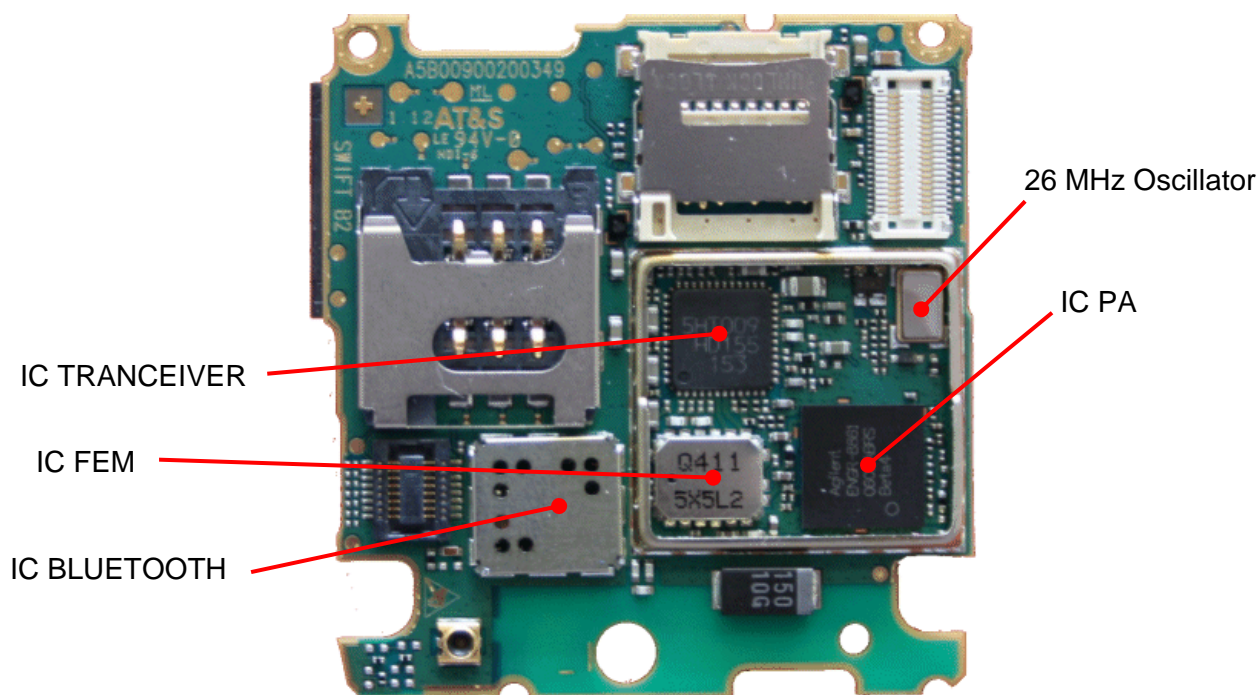
- Windows XP
- X-Focus version 2.22 or higher
- GRT Version 3.09 or higher
- Internet unblocking solution (JPICS)

## 5 PCB Main Board Overview

### PCB Main Board Top Side



### PCB Main Board Back Side





## 6 Radio Part

The radio part realizes the conversion of the GMSK-HF-signals from the antenna to the baseband and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

Transmitter and Receiver are never active at the same time. Simultaneous receiving in the GSM850/EGSM900 and GSM1800/GSM1900 band is impossible. Simultaneous transmission in the GSM850/EGSM900 and GSM1800/GSM1900 band is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

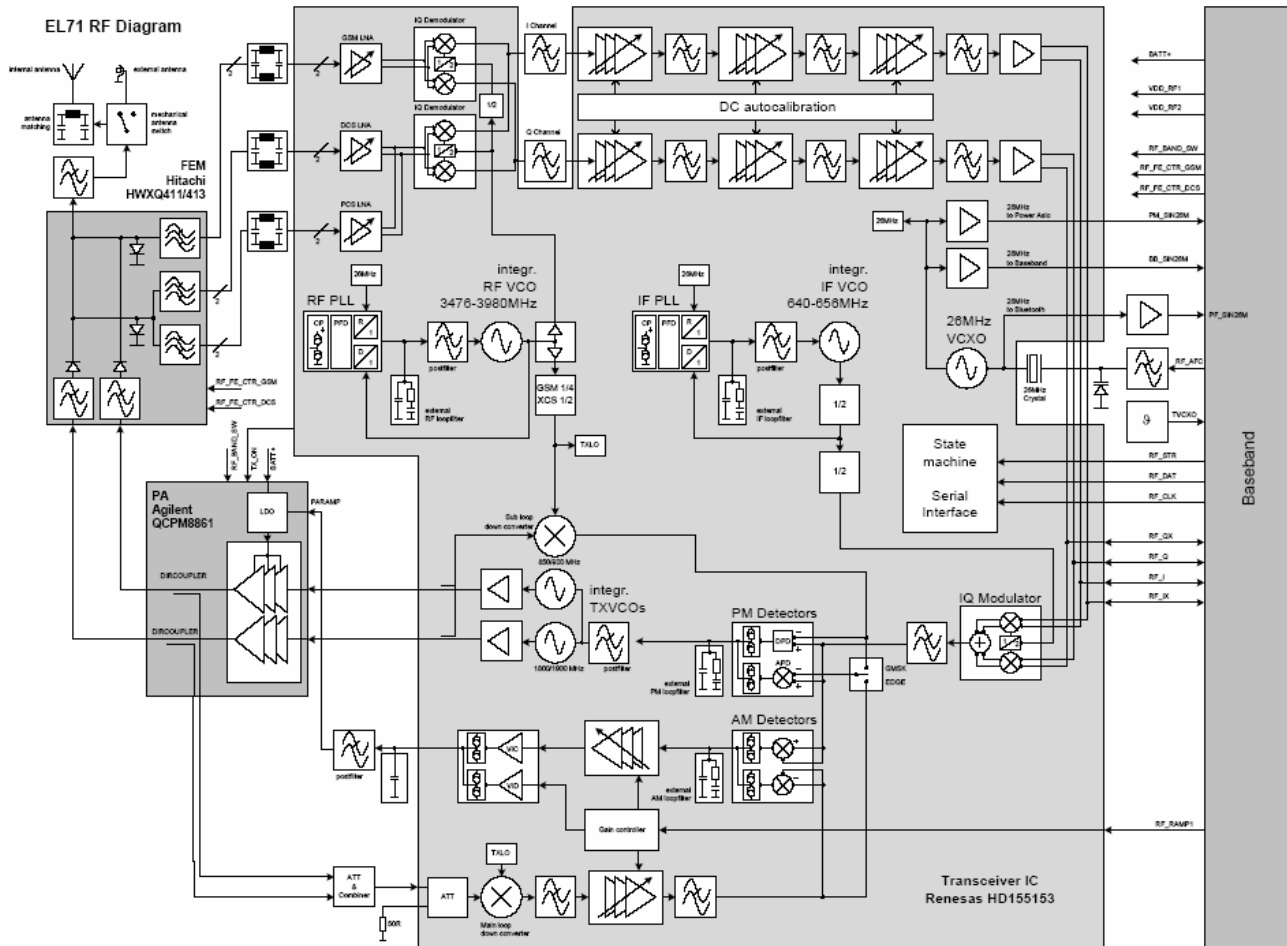
S75 RF-part is dimensioned for triple band operation (EGSM900, DCS1800, PCS19000) supporting GPRS functionality up to multiclass 10.

The RF-circuit consists of the following components:

- Renesas Bright 5PL chip set (HD155153NP) with the following functionality:
  - PLL for local oscillator LO1 and LO2 and TxVCO
  - Integrated local oscillators LO1, LO2 (without loop filter)
  - Integrated TxVCO (without loop filter and core inductors for GSM)
  - Direct conversion receiver including LNA, DC-mixer, channel filtering and PGC-amplifier
  - Active part of 26 MHz reference oscillator
  - Integrated Polar Loop, phase and amplitude control of transmitted output power
- Renesas LTCC transmit PA PF09026B (incl. integrated power control circuitry for GMSK mode)
- Frontend-Module including RX-/TX-switch and EGSM900 / DCS1800 / PCS 1900 receiver SAW-filters
- Crystal and passive circuitry of the 26MHz VCXO reference oscillator



## 6.1 Block diagram RF part

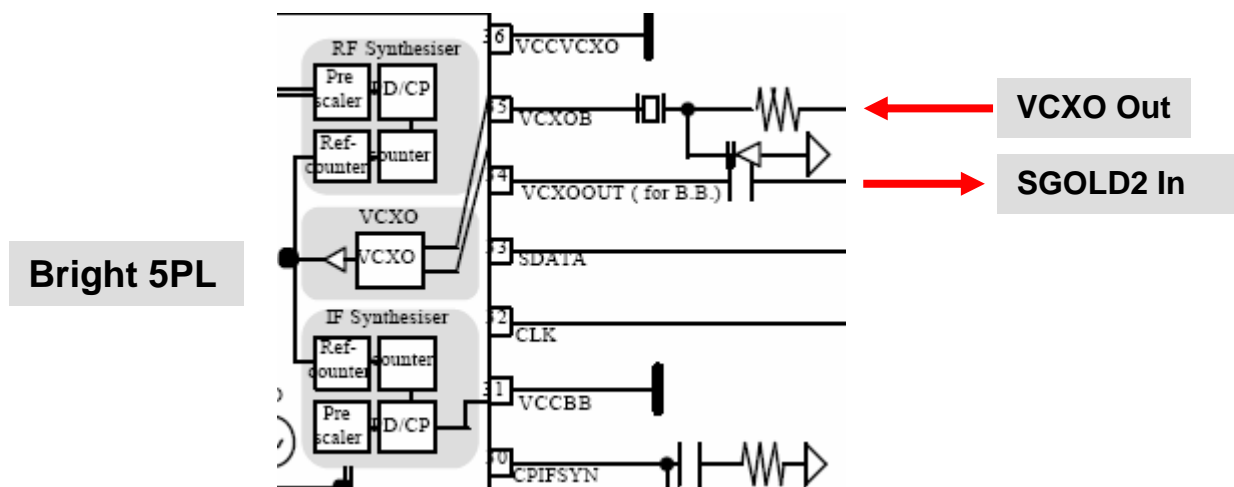


## 6.2 Power Supply RF-Part

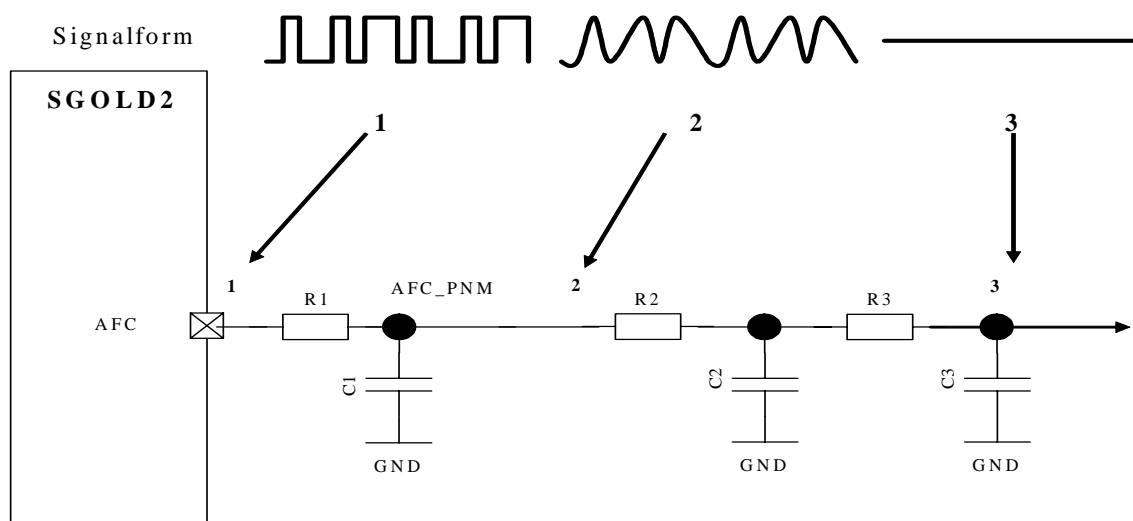
The voltage regulator for the RF-part is located inside the [ASIC D1300](#). It generates the required 2,8V "RF-Voltages" named **VDD\_RF1** and **VDD\_RF2**. **VDD\_RF2**. The voltage regulator is activated as well as deactivated via **VCXOEN\_UC** ([Functional K19](#)) provided by the [SGOLD2](#). The temporary deactivation is used to extend the stand by time.

### 6.3 Frequency generation

The 26 MHz signal is created by a discrete VCXO (Z3961). The active part is realised within the Bright. For temperature measurements of the VCXO a temperature sensor (R3967) is used. The frequency of the reference oscillator can be fine tuned by the SGOLD2 via a filtered PNM modulated AFC signal (RF\_AFC). Two active buffer stages are included in Bright 5PL to provide clock signals for the SGOLD2 (BB\_SIN26M) and the Power Supply ASIC (PM\_SIN26M). An additional external buffer (V3962) is used to deliver a 26MHz clock signal to the bluetooth chip (BT\_SIN26M).



The required voltage **VDD\_RF1** is provided by the ASIC **D1300**



Waveform of the AFC signal from **SGOLD2** to Oscillator

### Synthesizer: LO1

First local oscillator (LO1) consists of a PLL and VCO inside Bright (N3911) and an external loop filter (C3901, C3902).

#### RF PLL

The minimum frequency step is 400 kHz in GSM1800/GSM1900 mode and 800kHz in EGSM900 bands due to the internal divider by two for GSM1800/GSM1900 and divider by four for EGSM900. The PLL is controlled by the internal state machine which is connected to the SGOLD2 via tree-wire-bus. (RF\_DAT; RF\_CLK; RF\_STR)

#### RFVCO (LO1)

The first local oscillator is needed to generate frequencies which enable the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. The full oscillation range is divided into 16 sub bands and covers 3476 to 3980MHz. To do so, a control voltage for the LO1 is used, gained by a comparator. This control voltage is a result of the comparison of the divided LO1 and the 26MHz reference Signal. The division ratio of the dividers is programmed by the SGOLD2, according to the network channel requirements.

### Synthesizer: LO2

The second local oscillator (LO2) consists of a PLL and a VCO which are integrated in Bright 5PL (N3911) and a second order loopfilter which is realized external (C3940, C3941, R3952). Due to the direct conversion receiver architecture, the LO2 is only required for transmit operation in order to generate the transmit IF. To avoid inband spurious in the transmit signal the TX IF frequency is not fixed for the whole band. The LO2 covers a frequency range from 640 to 656MHz.

Before the LO2 signal enters the modulator it is divided by 8. So the resulting TX IF frequencies are 80/82 MHz. The complete LO2 operation is controlled by the Bright internal state machine.

The LO2 PLL and power-up of the VCO is controlled via the tree-wire-bus of Bright (SGOLD2 signals RF\_DAT; RF\_CLK; RF\_STR). To ensure the frequency stability, the 640MHz VCO signal is compared by the phase detector of the 2<sup>nd</sup> PLL with the 26Mhz reference signal. The resulting control signal passes the external loop filter and is used to control the 640/656MHz VCO.

The required voltage VDD\_RF1 is provided by the ASIC D1300

### Frontend-Module (FEM)

The frontend module (N3800) includes the RX/TX- and bandswitch function based on a combined PIN diode and diplexer-circuit. In the transmit paths a harmonic filtering for EGSM900 and GSM1800/GSM1900 is realized to avoid additional discrete filters. The isolation in TX OFF mode is used to achieve the isolation which is necessary before the active part of the burst. Two lines from the SGOLD2 control the band-selection of the TX switches (RF\_FE\_CTRL\_GSM, RF\_FE\_CTRL\_GSM). The three receiver chains include SAW filter for EGSM900, GSM1800 and GSM1900 to protect the receivers from strong blocking signals.

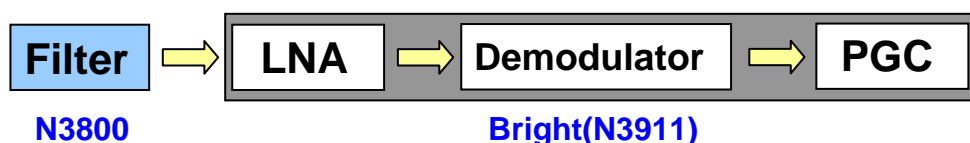
## 6.4 Receiver

### Receiver: Filter to Demodulator

The Bright 5PL incorporates three RF LNAs for EGSM900, GSM1800 and GSM1900 operation followed by direct conversion mixers which are IQ demodulators. The LNA/mixer can be switched in normal-, low- and lower-gain mode. For the "normal gain" state the mixers are optimised in terms of conversion gain and noise figure, in the "low gain" state the mixers are optimised for large-signal behaviour for operation at a high input power levels. The "lower gain mode" reduces the RF-level by activating a differential impedance in front of the LNA to improve the large signal performance.

Furthermore the IC includes a programmable gain baseband amplifier PGA (90dB control range, 2dB steps) with automatic DC offset calibration. The channel filtering is realized inside the chip with a four stage baseband filter for both IQ chains. Only two capacitors which are part of the first passive RC-filters are external (C3905, C3906). The second, third and fourth filters are active filters and are fully integrated. The distributed channel filter is necessary to suppress adjacent channel and inband-blocking interferer to avoid any compression in each amplifier stage.

The downconverted IQ signals are fed into the A/D converters inside the SGOLD2. By a special algorithm the level of the IQ signals is kept constant on a defined level by varying the PGA gain and selecting the appropriate LNA gains.



The required voltage **VDD\_RF1** and **VDD\_RF2** are provided by the ASIC **D1300**

## 6.5 Transmitter

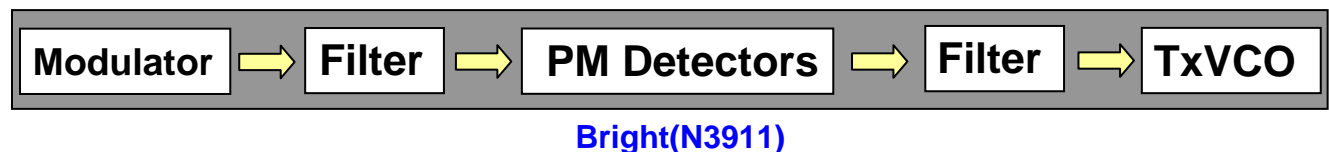
### Modulator

The generation of the modulated RF signal in Bright 5PL (N3911) is based on the principle of the polar loop architecture. The IQ signals generated by the SGOLD2 baseband are modulated to the transmit IF of 80MHz by an IQ modulator. The required carrier frequency is provided by the LO2.

As in a conventional upconversion loop the IF signal is upconverted to the transmit frequency. Therefore a downconverter and a phase detector are used in order to compare the IF signal to the downconverted transmit signal. This loop is called PM loop and is used for GMSK operation.

In 8PSK mode the 80MHz IF signal is split into PM and AM components. A second loop is then used to control the AM components. Therefore an AM detector is implemented which compares the 80MHz IF signal and the downconverted transmit signal. The AM loop is also used for power ramping. Inside the AM loop there are two analogue gain controlled amplifiers. These are used for setting the output power level and to keep the loop bandwidth constant.

The separated AM and PM components of an 8PSK signal are finally fit together inside the PA. The PA is driven by the TXVCO signals containing the PM components. The AM component is added by an amplitude control input pin, which controls the supply voltage of the RF transistors and therefore the PA output power level.

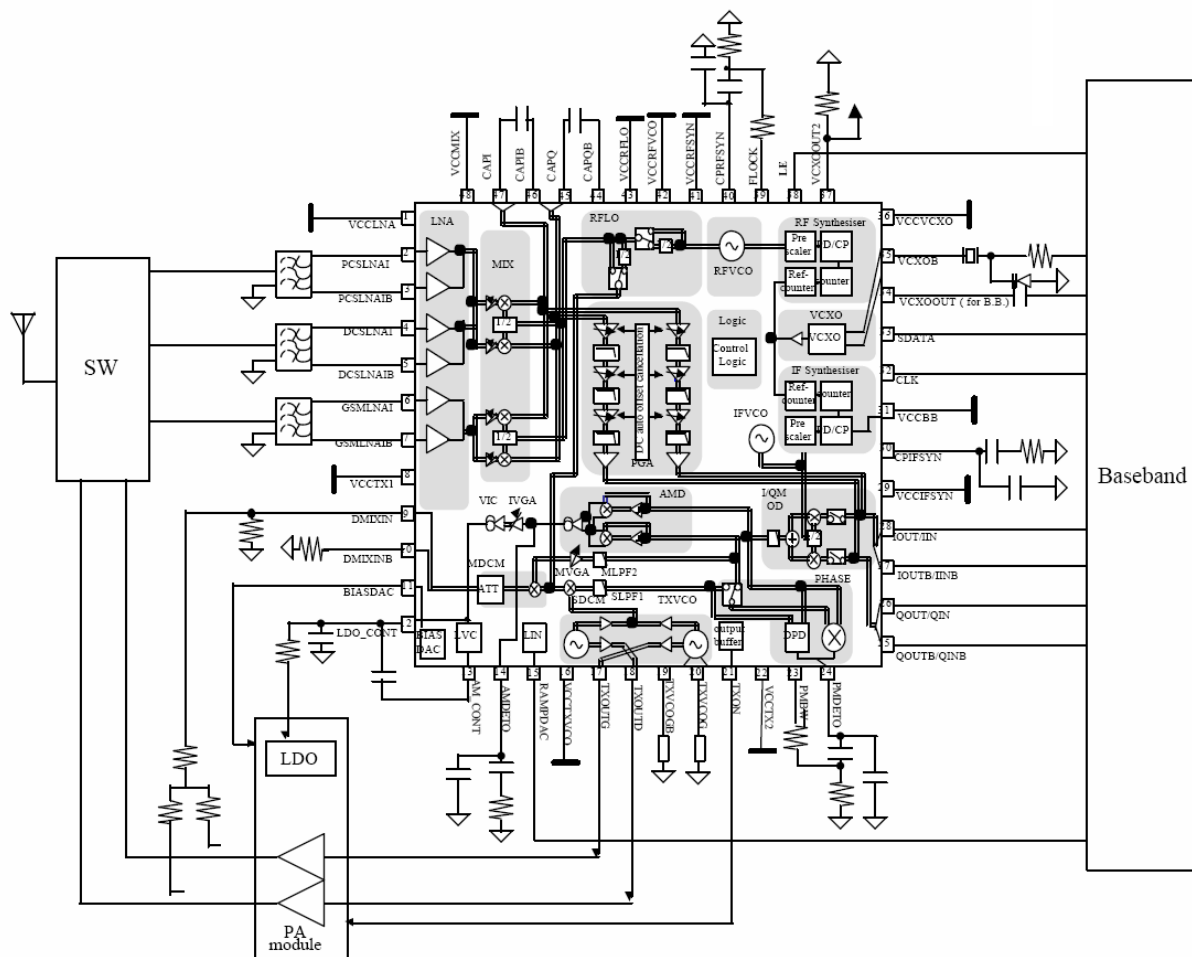


The required voltage **VDD\_BRIGHT** is provided by the ASIC D1300

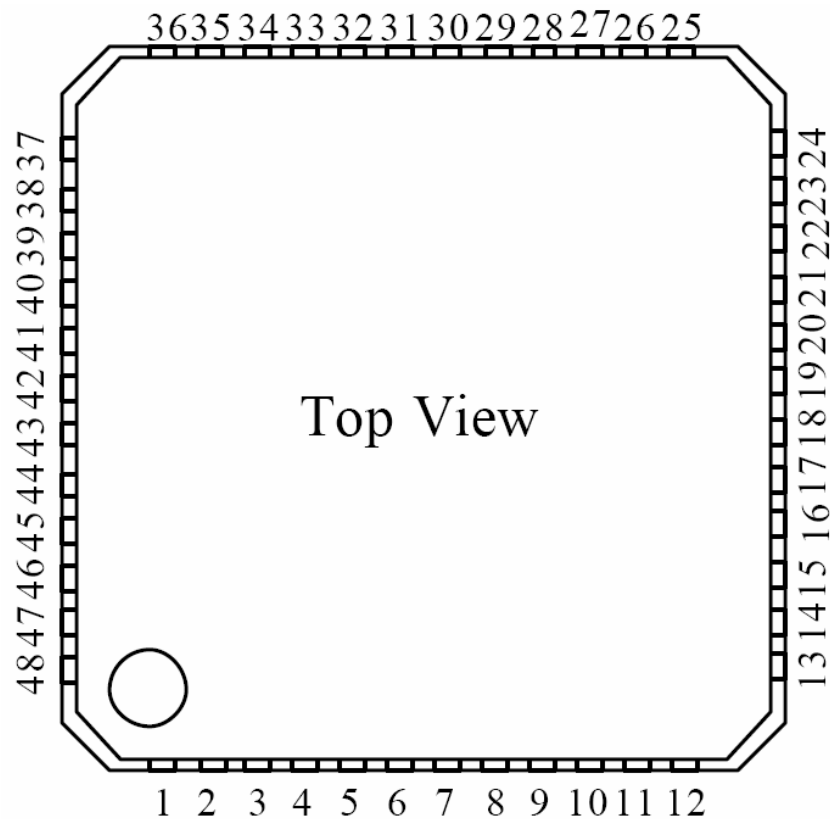
## 6.6 Bright IC Overview

BRIGHT 5PL

## IC Overview

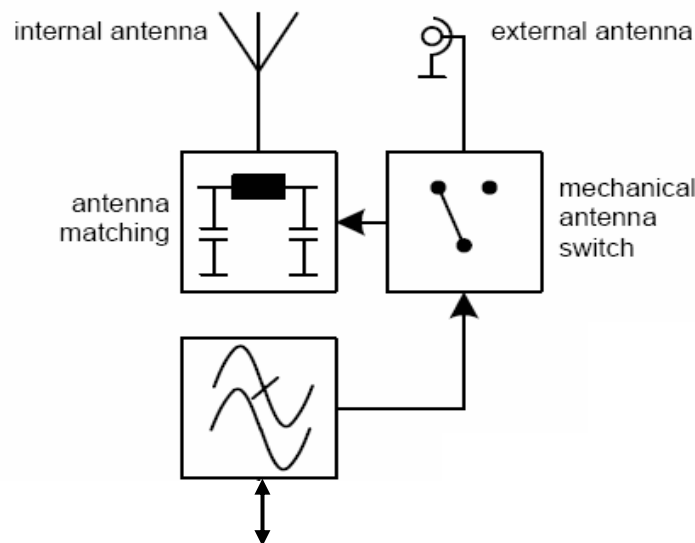


IC top view



6.7 Mechanical Antenna switch

The S75 mechanical antenna switch is used for the differentiation between the internal and external antenna.





## 6.8 Power Amplifier and Power Control

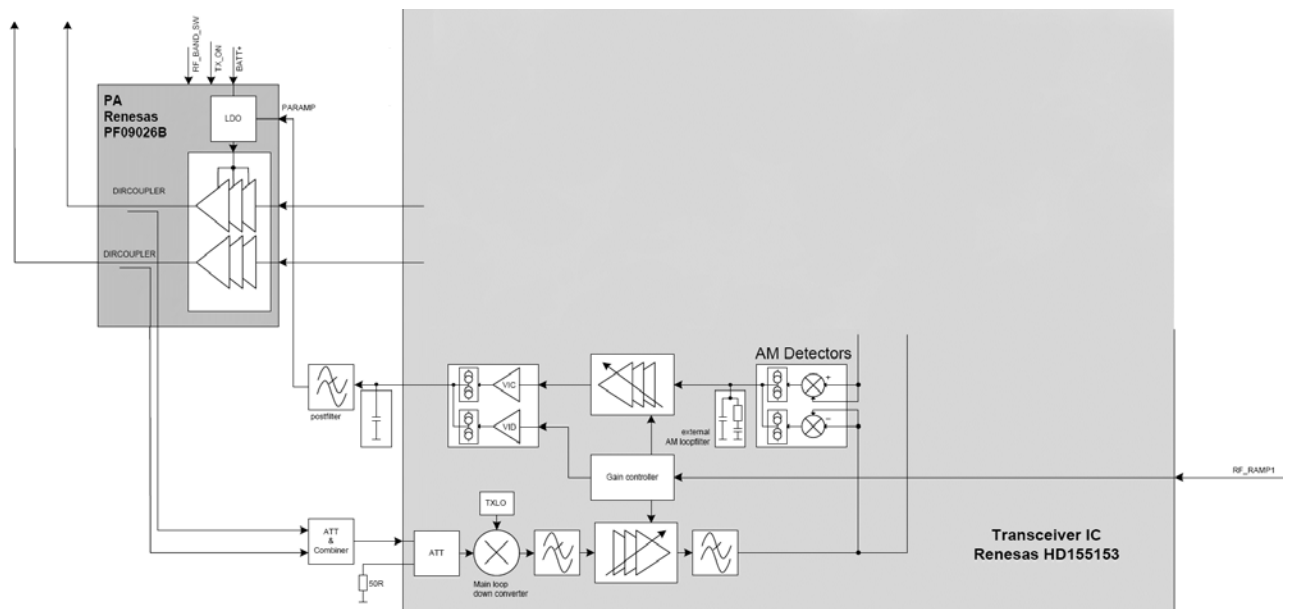
### PA

The power amplifier is a LTCC (Alumina-oxyd-ceramic) PA module, matched to  $50\ \Omega$  at all signal ports. It contains two separate 3-stage amplifier chains for EGSM900 and GSM1800/GSM1900 operation. It is possible to control the output power level of both bands via one VRAMP port. The appropriate amplifier chain is activated by a logic signal, which is provided by the **SGOLD2** (**RF\_BAND\_SW**). The module is switched on by a control signal generated by the **Bright5PL** internal state machine (**TX\_ON**). The RF transistor bias voltage is generated inside the PA module. The PA module consists also of two additional directional coupler, to provide the needed RF feedback signal for the AM control in 8PSK Mode.

The required voltage **BATT+** is provided by the battery.

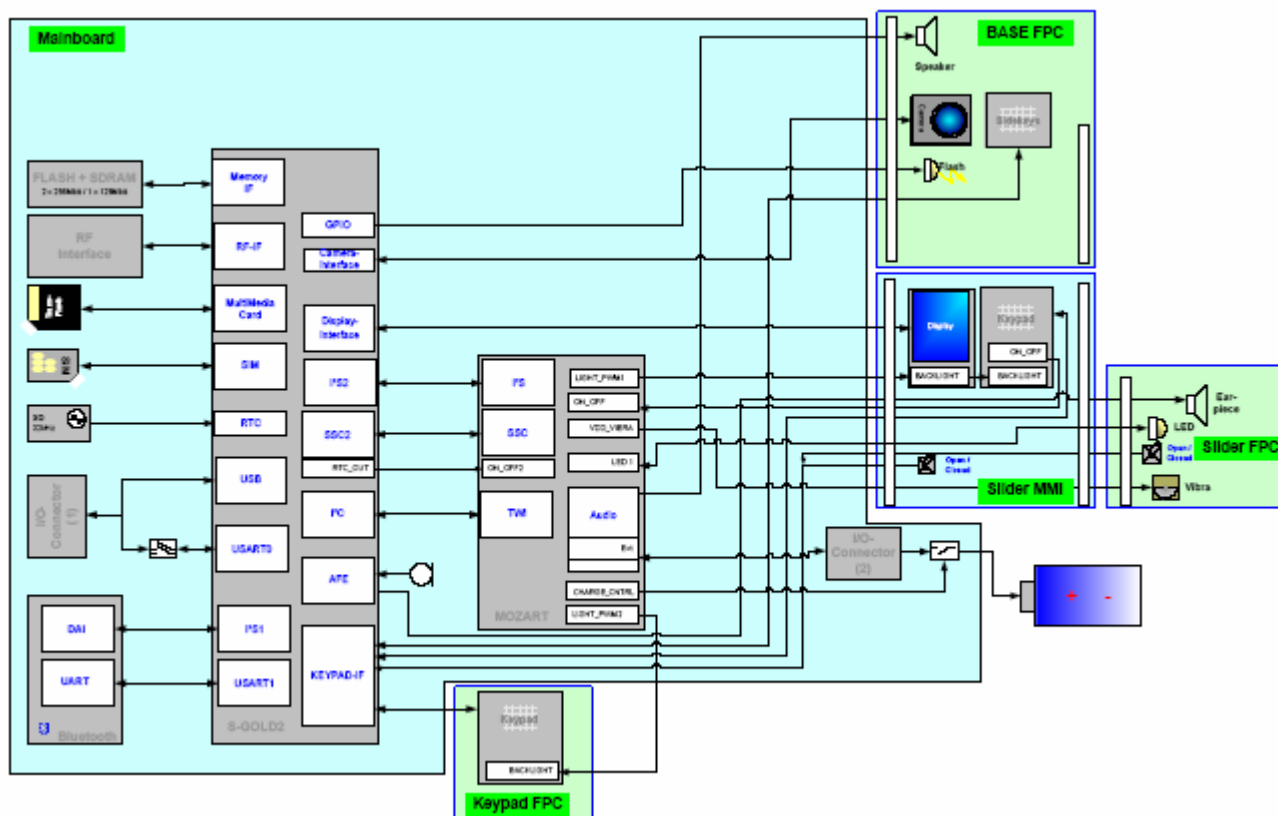
### Power Control

In GMSK operation the output power is directly controlled by a control voltage coming from **SGOLD2**. This voltage is fed through **Bright5PL** and connected to the PA module (**PARAMP**). In 8PSK operation the AM loop controls the output power level. Therefore the same **SGOLD2** signal is used but connected to the variable gain amplifiers inside **Bright5PL**. The AM control voltage finally controls the PA module (**PARAMP**). All switching between GMSK and 8PSK modes is controlled by the **Bright5PL** internal state machine.



## 7 Logic / Control

### 7.1 Overview Hardware Structure EL71



## 7.2 SGOLD2

### Baseband Processor SGOLD2 Features

#### Supported Standards

- EGPRS class 12 MCS 1..9
- GSM speech FR, HR, EFR and AMR-NB
- GSM data 2.4kbit/s, 4.8kbit/s, 9.6kbits, and 14.4kbit/s
- HSCSD class 10
- GPRS class 12 CS 1..4

#### Processing cores

- ARM926EJ-S 32 bit processor core with operating frequency up to 156 MHz for controller functions. The ARM926EJ-S includes an MMU, and the Jazelle Java extension for Java acceleration.
- TEAKLite® DSP core with operating frequency 138.67 MHz.

#### ARM-Memory

#### TEAKLite®-Memory (word: 16bit)

#### Shared Memory Blocks (word: 16bit)

#### Controller Bus System

#### TEAKLite® Bus System

#### Clock System

The clock system allows widely independent selection of frequencies for the essential parts of the S-GOLDlite™. Thus power consumption and performance can be optimized for each application.

#### Functional Hardware blocks

- CPU and DSP Timers
- Programmable PLL with additional phase shifters for system clock generation
- GSM Timer Module that off-loads the CPU from radio channel timing
- GMSK Modulator according to GSM-standard 05.04 (5/2000)
  - GMSK Modulator: gauss-filter with  $B \cdot T = 0.3$
- Hardware accelerators for equalizer and channel decoding
- A5/1, A5/2, A5/3 Cipher Unit  
(A5/3 added in S-GOLDlite™ V1.1)
- GEA1, GEA2, GEA3 Cipher Unit to support GPRS data transmission  
(GEA3 added in S-GOLDlite™ V1.1)
- Advanced static and dynamic power management features including TDMA-Frame synchronous low-power mode and enhanced CPU modes (idle and sleep modes)
- Incremental Redundancy Memory for EDGE class 12 support
- GMSK / 8-PSK Modulator according to GSM-standard 05.04 (5/2000)
  - GMSK Modulator: gauss-filter with  $B \cdot T = 0.3$
  - EDGE Modulator: 8PSK-modulation with linearised GMSK-pulse-filter
- MOVE coprocessor performing motion estimation for video encoding algorithms (H.263, MPEG-4)

**Signal Processing Firmware Support**

- FR, HR, EFR, and AMR
- data transmission channel codecs for 2.4, 4.8, 9.6 and 14.4 kbit/s
- HSCDS class 10 support
- GPRS class 12 support with coding schemes CS1..4
- Support for Handsfree, side- and signaling tone generation
- MMS-support
- EGPRS class 12 with modulation and coding schemes MCS1..9 (Release 5 compliant)
- Polyphonic ringer for up to 64 voices at sampling rates up to 48kHz
- 64 voices midi (pseudo) stereo
- enhanced audio visualization
- voice control

**Interfaces and Features**

- Keypad Interface for scanning keypads up to 8 rows and 8 columns
- Pulse Number Modulation output for Automatic Frequency Correction (AFC)
- Serial RF Control Interface; support of direct conversion RF
- 2 USARTs
- IrDA Controller
- 1 Serial Synchronous SPI compatible interfaces in the controller domain
- 1 Serial Synchronous SPI compatible interface in the TEAKLite® domain
- I2C-bus interface
- 2 bidirectional and one unidirectional I2S interface accessible from the TEAKLite®
- USB V1.1 mini host interface
- IEEE 1149.1 compliant JTAG port for Boundary Scan and debug
- ISO 7816 compatible SIM card interface
- Enhanced digital (phase linearity, adj/ co-channel interference) baseband filters, including analog prefilters and high resolution analog-to-digital converters.
- Digital and analog audio filters including wideband audio capable digital-to-analog and analog-to-digital converters.
- Audio front-end will be accessible from MCU (via shared memory) and the TEAKLite® (i.e. voice recognition and echo cancellation can run on TEAKLite®)
- Hifi Stereo voiceband with CD-Quality
- Separate analog-to-digital converter for various general purpose measurements like battery voltage, battery, VCXO and environmental temperature, battery technology, transmission power, offset, onchip temperature, etc.
- Ringer support for highly oversampled PDM/PWM input signals for more versatility in ringer tone generation
- Differential VMIC generation
- RF power ramping functions
- DAI Interface according to GSM 11.10 is implemented via dedicated I2S mode
- 26 MHz master clock input
- External memory interface:
- Port logic for external port signals
- Comprehensive static and dynamic Power Management
  - Various frequency options during operation mode
  - 32 kHz clock in standby mode
  - Sleep control in standby mode
  - RAMs and ROMs in power save mode during standby mode
- Debug Features

- 2 General Purpose Timers with 3 32-bit timers
- Serial number
- A real time clock with alarm functions
- 2 capture/compare units with 16 channels
- A fast parallel Display Interface
- Camera Interface
- Programmable clock output for a camera
- An Multimedia/Secure Digital Card Interface (MMCI/SD; SDIO capable)
- A Flash Controller DMA Port (FCDP) supporting NAND flash
- A multimedia extension interface (MMIC-IF) supporting external hardware accelerator
- A Fast IrDA Interface
- A Universal Serial Interface (USIF) enabling asynchronous or synchronous serial data transmission.

### 7.3 SDRAM

The SDRAM (Synchronic Dynamic Random Access Memory) is for volatile data.

Memory Size:	128 Mbit (16 MByte)
Data Bus:	16Bit
IO / Core Voltage Supply:	typ. 1.8 V

### 7.4 FLASH

It is a non-volatile-, re-programmable- memory (SW-updateable), with a high performance interface. The mobile-SW can be executed directly. The Flash has an unchangeable serial number.

#### Intel Sibley:

Memory Size:	512 Mbit (64 MByte)
Data Bus:	16 Bit
IO / Core Voltage Supply:	typ. 1.8V

### 7.5 SIM

SIM cards with supply voltages of 1.8V and 3V are supported..

### 7.6 Vibration Motor

The vibration motor is mounted in the lower case of the base part. The electrical connection to the PCB is realised with pressure contacts.

## 8 Display

In the S75 a display module with an intelligent graphic Liquid Crystal Display (LCD) is used. The display module consists of the following parts and features

- an Active Matrix Liquid Crystal Display Panel, 132x176 dots, 262k colors, positive mode
- a display controller mounted on the display glass which is connected to a FPC inside the module
- a light guide with 4 white LED's
- Illumination foil stack is implemented in the module
- A PCB/FPC with all passive components.
- An electrical interface that consists of land pattern designed for spring connector. The 20-pin spring connector is mounted on the PCB
- Parallel 8-bit interface

## 9 Camera

The camera module consists of a 1.3MPix-CMOS sensor, image processor circuitry, lens and holder, lens hood, cover glass and housing to attach the camera on the PCB. Connectivity from camera module to PCB is realized by using a socket.

## 10 Bluetooth

The Bluetooth Interface [BRF6150](#) is compatible to the Bluetooth specification version 1.2 power class 2 (-6 dBm up to +4dBm) with a RX sensitivity better than -70 dBm and support multipoint connections.

It supports a transmission rate up to 723 kBit/s data asymmemetrically over the air interface.

The transmission range is approx. 10 m. Between SGOLD2 and BRF6150 a data rate up to 4921.6 8 kbit/s is used.

The following table shows the interface between [SGOLD2](#), [ASIC](#) and the [BRF6150](#)

Pin name		Signal name	Meaning	Connected to
VDD_IN_BB VDD_IN_RFIO VDD_IN_ANA VDD_IN_OSC	IN	VDD_BT VDD_BT_RF2	Main power supply	ASIC "VREF3"
VDD_IO_x VDD_IO_SF_x	IN	2.65V 2.65V (2.9V)	IO Power supply 2.9V needed for stacked flash	ASIC VDD IO SGOLD REG3 2.65V (REG1 2.9V)
HCI_RTS	OUT	BT_CTS	USART IF	SGOLD2 "USART1_CTS"
HCI_RX	IN	BT_TX	USART IF	SGOLD2 "USART1_TX" or SGOLD2 "USIF_TXD_MSTR"
HCI_TX	OUT	BT_RX	USART IF	SGOLD2 "USART1_RX" or SGOLD2 "USIF_TXD_MSTR"
HCI_CTS	IN	BT_RTS	USART IF	SGOLD2 "USART1_RTS"
AUD_CLK	IN	BT_PCM_CLK	PCM IF	SGOLD2 "I2S1_CLK"
AUD_FSYNC	IN	BT_PCM_SYNC	PCM IF	SGOLD2 "I2S1_WA0"
AUD_IN	IN	BT_PCM_IN	PCM IF	SGOLD2 "I2S1_TX"
AUD_OUT	OUT	BT_PCM_OUT	PCM IF	SGOLD2 "I2S1_RX"
HCI_TX	OUT	BT_WAKEUP_GM	Wakeup-line, needed if H5 is not used	SGOLD2 "KP_IN6"
NSHUT_DOWN	IN	BT_RESET	Reset	ASIC "Outport"
CLK32	IN	CLK32	32,768 kHz +-250ppm Rectangular wave	S-GOLD2 "CLK32"
XTALP_FAST_ CK_IN	IN	BT_SIN26M	26MHz clock signal sine wave	RF-GSM
IO0_EXT_CLK_ REQ_OUT	OUT	BT_VCXOEN	26MHz clock request	ASIC "SLEEP2N"



## 11 Power Supply

### 11.1 ASIC Mozart / Twigo4

The power supply ASIC will contain the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the uC with a watchdog
- 17 Voltage regulators
- 2 internal DC/DC converters (Step-up(not used) and Step-down converter)
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI Interface (I<sup>2</sup>C interface)
- Bandgap reference
- High performance audio quality
- Audio multiplexer for selection of audio input
- Audio amplifier stereo/mono
- 16 bit Sigma/Delta DAC with Clock recovery and I<sup>2</sup>S Interface

### 11.1.1 Battery

As s standard battery a Li-ion battery with the nominal capacity of 630 mAh @ 0.2 CA \* and GSM capacity \*\* of minimal 600 mAh will be provide.

\* 0.2CA means battery pack will be discharged at 20% of capacity rate till 3.0V; e.g. 600mAh,  $0.2 \times 600 \text{ mA} = 120 \text{ mA}$ .

\*\* battery pack will be discharged at the pulse mode with 2A (0.6 ms) + 0.25A (4.0ms) till 3.2V.

### 11.1.2 Charging Concept

#### 11.1.2.1 General

The battery is charged in the phone. The hardware and software is designed for Lilon with 4.2V technology. Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging shall take place in the background (the customer can see this via the "Charge" symbol in the display). During normal use the phone is being charged (restrictions: see below).

Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The processor takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the PMU hardware can override/interrupt the charging in the case of over voltage of the battery

For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22k $\Omega$  at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. Charging is ongoing as long the temperature is within the range 0°C to 50°C. The maximal charge time will be 2 hours ( $I_{\text{max}}=750\text{mA}$ ).

#### 11.1.2.2 Measurement of Battery voltage, Battery Type and Ambient Temperature

The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the S-GOLDlite. Inside the S-GOLDlite are some analog to digital converters. These are used to measure the battery voltage, battery code resistor, the voltage at battery code capacitor and the ambient temperature.

#### 11.1.2.3 Timing of the Battery Voltage Measurement

Unless the battery is being charged, the measurement shall be made in the TX time slot. During charging it will be done after the TX time slot.

#### 11.1.2.4 Recognition of the Battery Type

The different batteries will be encoded by different resistors within the battery pack itself.

#### 11.1.2.5 Charging Characteristic of Lithium-Ion Cells

Lilon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is given by the connected charger. The battery voltage may not exceed 4.2V  $\pm 50\text{mV}$  average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be performed is in the ranges from 0...50°C. Outside this range no charging takes place, the battery only supplies current.

### 11.1.2.6 Trickle Charging

The ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will be measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the ASIC by means of the external FET. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.2V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the ASIC will switch on the phone automatically and normal charging will be initiated by software.

### 11.1.2.7 Normal Charging (Fast charge)

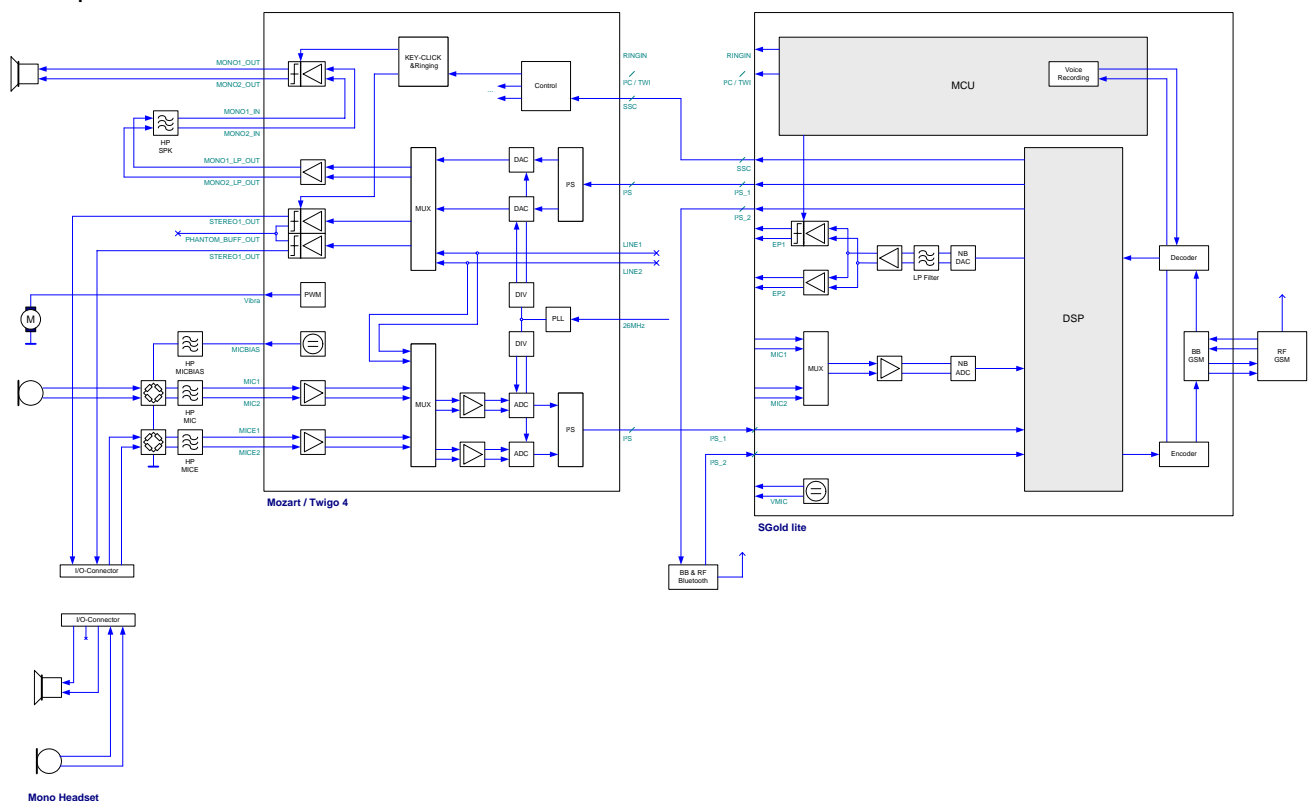
For battery voltages above 3.2 Volt and normal ambient temperature between 0 and 50°C the battery can be charged with a charge current up to 1C. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the ASIC. The level of charge current is only limited by the charger.

### 11.1.2.8 USB Charging

The ASIC can support USB charging when USB charging is integrated in the charging software. If charge voltage is in the range 4.4V to 5.25 V USB charging is ongoing. During USB charging only limited charging is possible. Charge current is limited to 75, 150, 300 or 400 mA.

### 11.1.2.9 Audio multiplexer

The digital audio information from/to the DSP inside the **SGOLD2** are delivered via the I2S interface, the 26MHz from the RF part. The internal AD and DA converter are connected to microphone and loudspeaker.



#### 11.1.2.10 Interface

The ASIC has two serial control interfaces and one serial audio interface. With the serial interfaces, all functions of the ASIC can be controlled. For time critical commands ( all audio functions incl. Vibra) the SSC is used.

##### **TWI interface**

TWI (two wire interface) is an I2C 2 wire interface with the signals Clock (**I2C\_CLK**) data line (**I2C\_DAT**) and the interrupt (**PM\_INT**).

##### **SSC interface**

The SSC interface enables high-speed synchronous data transfer between SGOLD and ASIC.

The interface consist of: clock signal (**PM\_SSC\_SCLK**), master transmit slave receive (**PM\_SSC\_MTSR**), master receive slave transmit (**PM\_SSC\_MTSR**) and the select line (**PM\_SSC\_CS**)

##### **IS2 interface**

The audio interface is a bidirectional serial interface, TX and RX part are independent. The IS2 interface consist of a three wire connection for each direction. The three lines are clock (CLK), the serial data line (DAC or ADC) and the word select line (WAO). Clock and word select line is used for RX and TX together in SL65. (**PM\_I2S\_DAC** for RX and **PM\_I2S\_ADC** for TX)

### 11.1.2.11 Voltage Regulators and DC/DC converters

#### Mozart Power Supplies

	Voltage	Current [mA]	start up default	ON/OFF by	Power supply name EL71	Domain
REG 1	2,9V (+/-2%)	0...140	on	I2C	2.9V	SGOLD, Display
	2,65V (+/-2%)					
REG 2a	1,5V (+/-2%) 1,3V...1,5V in 100mV steps	0...300	on		1.5V_UC	not used
REG 2b	1,5V (+/-2%) 1,3V...1,5V in 100mV steps	0...100	on	I2C	1.5V_DSP	not used
REG 3	2,65V (+/-2%)	0...140	on		2.65V	SGOLD, Bluetooth, Hall Switch, Audio/Video Interface
	2,5V (+/-2%)					
MEM REG1	1,8V (+/-2%)	0...250	on	I2C	1.8V_MEM1	SGOLD, Flash/SDRAM, Audio/Video Interface
	2,5V (+/-2%)					
MEM REG2	1,8V (+/-2%)	0...150	on	I2C	1.8V_MEM2	Flash/SDRAM
	2,5V (+/-2%)					
AUDIO REGa	2,9V (+/-2%)	0...190	off	I2C	VAUDREGA	internal use
AUDIO REGb	2,65 (+/- 2%)	0...30	off	I2C	n/a (Mozart internal use)	internal use
RF REG1	2,74V (+/-2%)	0...150	Sleep1_N or Sleep2_N	I2C	VDD_RF1	RF Tranceiver
	2,54V (+/-2%)					
	2,85V (+/-2%)					
RF REG2	1,53V (+/-2%) (CA Version)	0...180mA	depends on RF2_EN input	I2C	VDD_RF2	RF Tranceiver
	2,7V (+/-2%)					
	2,85V (+/-2%)					
RF REG3	1,8V (+/-2%)	0...180	depends on RF3_EN input	I2C	VDD_BT	Bluetooth
	2,7V (+/-2%)					
	2,85V (+/-2%)					
AFC REG	2,65V (+/-2%)	0...2	always active	n.a.	VDD_AFC	SGOLD
LP_REG	2,0V	0...2	always active	n.a.	VDD_RTC	SGOLD
SIM REGa	2,9V (+/-2%)	0...70	off	I2C	VDD_SIM	SIM
	1,8V (+/-2%)					
SIM REGb	2,9V (+/-2%)	0...10	on	I2C	n/a (not used)	not used
	1,8V (+/-2%)					
USB REG	3,1V (+/-2%)	0...40	on	I2C	VDD_USB	SGOLD
VIBRA	2,8V (+/-2%)	0...140	off	I2C	VDD_VIBRA	Vibra
DCDC STEP DOWN (BUCK-Converter)	1,5V	700	on	I2C	VBUCK	SGOLD
	2,1V					

## 11.2 External stepup converter

The stepup converter **N1300** supplies the LED for video/torchlight and flash light. It is also used to supply the display and keypad backlight LEDs. The converter is only capable to drive one of the above mentioned modes.

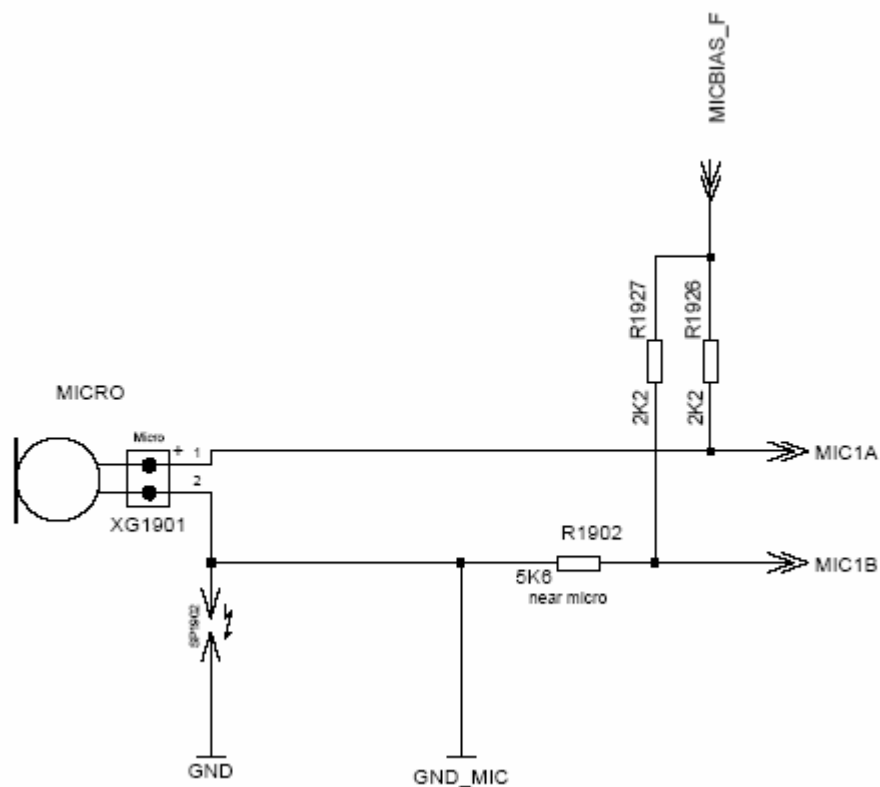
- Video/torchlight supply:  $V_{OUT} = 19,7V-20,7V$ ;  $I_{OUT} = 8,3mA$
- LED flash supply:  $19,7V-20,7V$ ;  $I_{OUT} = 65mA$ ; 400ms; Duty Cycle 1/10
- Display and Keypad backlight:  $19,7V-20,7V$ ;  $I_{OUT} = 30mA$

### Non Mozart power supplies

	Voltage	Voltage option change per	Current [mA]	start up default	ON/OFF by	Power supply name Swift	Domain
<b>BOOST-Converter: LM2733</b>	19,7V	ext. Resistor divider	60mA for 400ms 30mA continuos	off	SHDN pin	VBOOST	Flash-LED, Keypad backlight, Display backlight
<b>LDO: LP3985ITLX-2.9</b>	2,9V	n/a	150	off	VEN pin	DVDD_CAMERA	Camera
<b>LDO: LP3985ITLX-2.9</b>	2,9V	n/a	150	off	VEN pin	MMC_VCC	MicroSD card

## 12 Interfaces

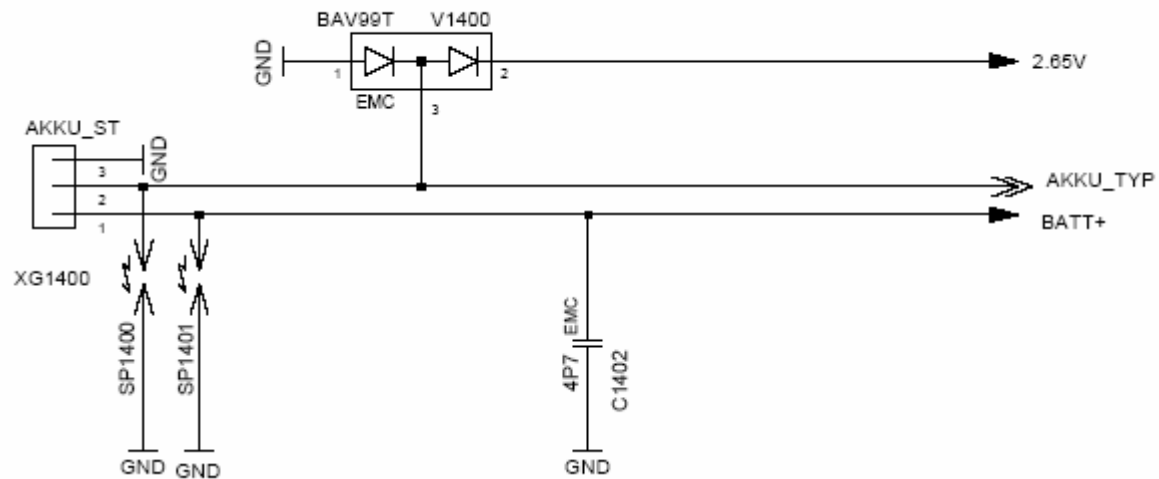
### 12.1 Microphone (XG2001)



Pin	Name	IN/OUT	Remarks
1	MIC1A	O	Microphone power supply. The same line carries the low frequency speech signal.
2	MIC1B		GND_MIC

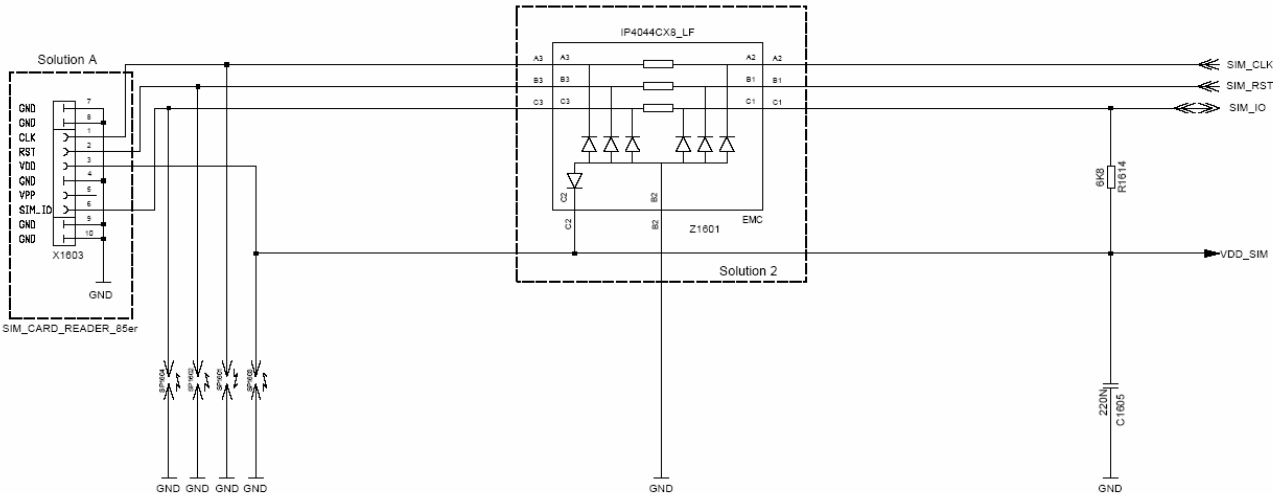


## 12.2 Battery (XG1400)



Pin	Name	Remarks
1	BATT+	Positive battery pole
2	AKKU_TYP	Recognition of battery/supplier
3	GND	Ground

12.3Interface SIM Module with ESD protection



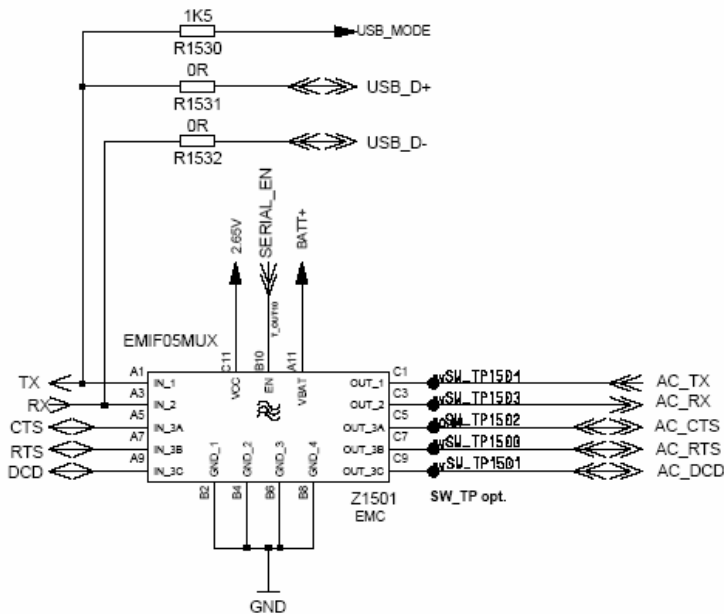
Pin Name	IN/OUT	Remarks
SIM_CLK	O	Pulse for chipcard. The SIM is controlled directly from the SGOLD.
SIM_RST	O	Reset for chipcard
SIM_IO	I/O	Data pin for chipcard
VDD_SIM	O	Switchable power supply for chipcard;

The [Z1601](#) is a 3-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals. Additionally diodes are contained to protect downstream components from Electrostatic Discharge (ESD) voltages



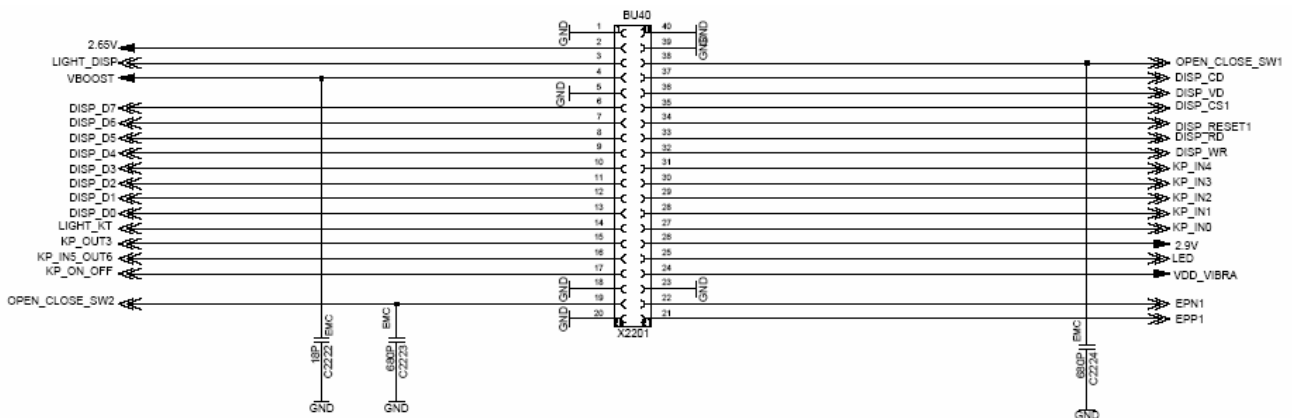
## ESD Protection with EMI filter

The **Z1501** is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band. Additionally, the **Z1501** contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages.



## 12.5 Board to Board Connector (Display/Slider)

Display, Vibra, Loudspeaker, Keyboard and keypad illumination are connected via an board to board connector (**X2201**).



### 12.5.1 Interface of the display module.

All displays need a supply voltage of  $VDD_{2.9} = 2.90\text{ V}$ .

Four white side-shooter LEDs for illumination are mounted on the module FPC. The current for the LEDs is limited to max. 18mA. All four LEDs are in serial.

For data transmission there is used an 8-bit parallel interface with a maximum transfer-rate of 10 MHz. To avoid tearing effects during data transmission a synchronization signal is available on pin "LCD-sync".

Pin Number	Pin Name	Description
1	LCD_D7	Parallel 8bit data IF D7 (MSB)
2	LCD_D6	Parallel 8bit data IF D6
3	LCD_D5	Parallel 8bit data IF D5
4	LCD_D4	Parallel 8bit data IF D4
5	LCD_D3	Parallel 8bit data IF D3
6	LCD_D2	Parallel 8bit data IF D2
7	LCD_R	Read, active at falling edge
8	LCD_WR	Write (Clock), active at rising edge
9	LCD_GND	Ground
10	LCD_SYNC	Picture Sync against Tearing Effect
11	LCD_LED_A	Supply Voltage LED+
12	LCD_LED_C	Supply Voltage LED-
13	LCD_CS	Chip Select, low active
14	VDD_IO	Supply Voltage I/O 1,8Vtyp.
15	VDD_LCD	Supply Voltage LCD 2,9Vtyp
16	LCD_RS	Data=high/Command=low
17	LCD_GND	Ground
18	LCD_D0	Parallel 8bit data IF D0 (LSB)
19	LCD_D1	Parallel 8bit data IF D1
20	LCD_RESET	Reset; low active

### 12.5.2 Illumination

The 4 serial LEDs for the display are supplied by one constant current source, to ensure the same brightness and color of the white backlight. The illumination of the display is coupled with the illumination of the Slider-Keypad.

### 12.5.3 SLI-LED

Due to the fact that the display will be switched off in StandbyMode for power saving reasons a signaling LED is used for indicating that the device is switched on and working or any other action has occurred (incoming call, network lost, download ongoing, etc.). The color is green. The Led is switched on by the SGOLD2 via a switching transistor. The blinking frequency is adjustable by SW.

### 12.5.4 Base Keyboard

The Base-Keypad matrix consists of the keys "0" to "9", "\*", "#". They are located on a (F)lexible(P)rinted(B)oard which is connected to the main board by a 14-pin-Connector.

### 12.5.5 Slider Keyboard

The Slider-Keypad matrix consists two soft keys, a 5-way-navy-key, a "SEND"-, an "END"-, a "Direct Line" and a "Media Player"-key. They are placed on a PBC which is connected to the main board via the Slider-FPC. The "END"-Key has a double-function. If the mobile phone is switched off the "END"-key is supported by a resistor with RTC-Voltage.

### 12.5.6 Side Keys

In addition, four side keys (two rocker keys on each side) are connected to the matrix. They are located on the camera-FPC.

### 12.5.7 Keypad Illumination

Opal black phones: 6x white LEDs (top shooter) driven by max. 5mA / LED

Quartz anthracite and Azurite Silver phones: 8 x blue (top shooter) driven by max. 5mA / LED

The illumination of the Slider-Keypad will be done via 4 high brightness LEDs in serial; color: white, type: top-shooter, driven by max. 5mA / LED).

## 12.6 RSMMC Reader

The memory card is controlled by the MMC/SD interface of the SGOLD2. The new card type is called MicroSD. Currently commercially available is the Transflash™ Card. The SD-card interface is based on the MMC-card interface with three signals MMC\_CMD, MMC\_DAT, MMC\_CLK. The Data bus of the SD card could be switched to 4-Bit mode if higher data rates are required. This feature is not used in the current design.

#### SPI mode

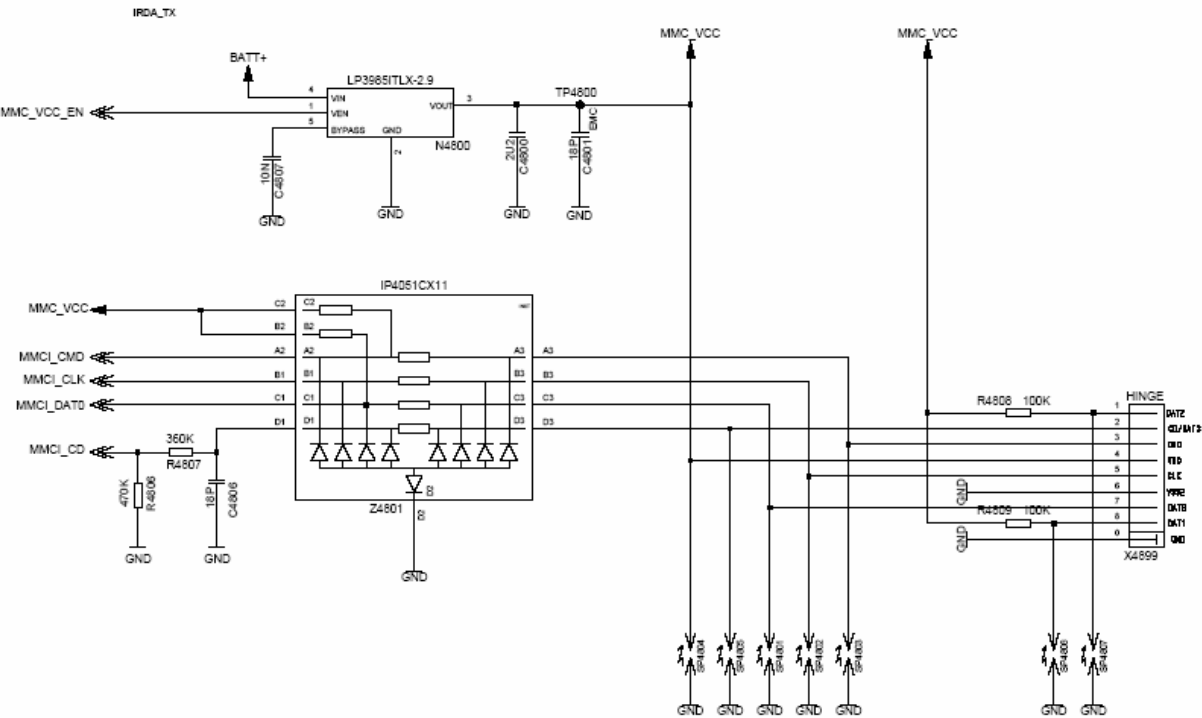
The MMC-interface of SD/MMC cards can be switched into SPI mode with the first initialization command. In order to prevent the card from switching into SPI mode, the level on Pin2 (CD/DAT3) of the card must be high during the initialization. We use a pull up resistor on this pin.

#### MMC interface and signal characteristics

Signal	Direction at MMC	Driver type
DAT0	Bi-directional	Push-pull
CMD	Bi-directional	Push-pull/open-drain
CLK	Output	Push-pull

#### Card detection

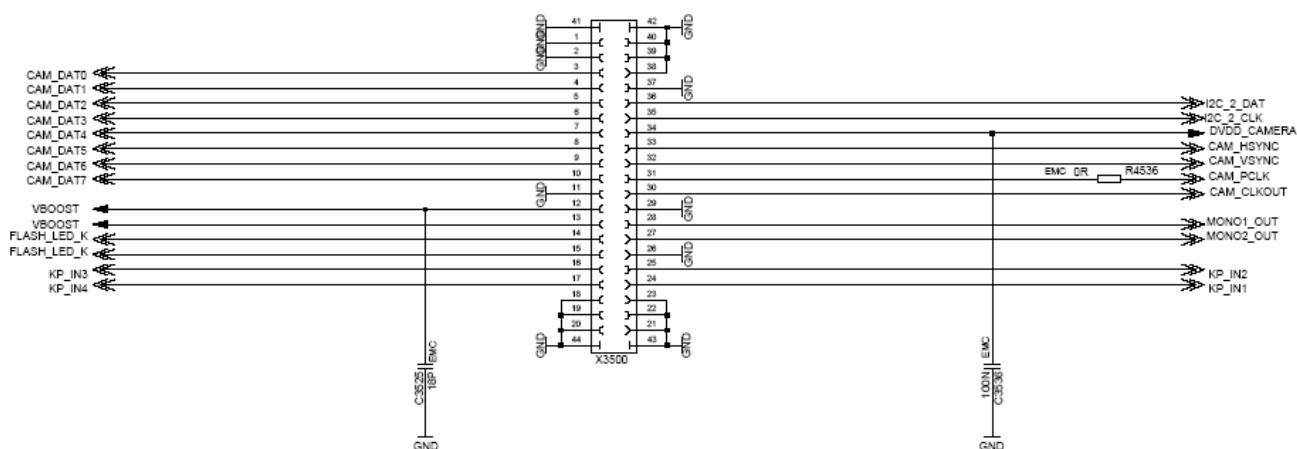
An internal pull up resistor of the card on Pin 1 (DAT2) in combination with an external pull down resistor. When the card is inserted and powered, we get a high signal on the external pull down resistor which creates a state change on a SGOLD2 GPIO. A simple RC-Low pass Filter is used on the detection signal for de-bouncing.



Signal	Function	Direction at MMC
MMC_DAT	Data	Bi-directional
MMC_CMD		Bi-directional
MMC_CLK	Clock	Output
MMC_VCC	Power supply	Input
GND	GND	



## 12.7 Camera Interface

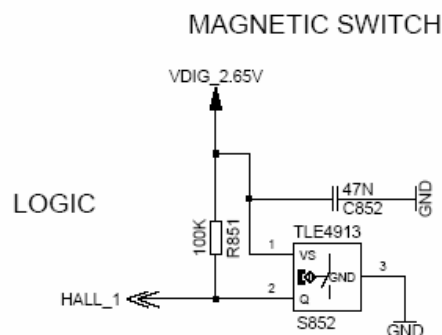


Pin Number	Pin Name	Description	I/O <sup>i</sup>
01	GND	Ground	N/A
02	EXCLK	Camera Clock	O
03	GND	Ground	N/A
04	Pixel Clock	Pixel Data Clock	I
05	GND	Ground	N/A
06	SDA	I2C Data	I/O
07	SCL	I2C Clock	O
08	GND	Ground	N/A
09	H_SYNC	Horizontal Synchronization	I
10	V_SYNC	Vertical Synchronization	I
11	GND	Ground	N/A
12	Data 7	Data bit 7	I
13	Data 6	Data bit 6	I
14	Data 5	Data bit 5	I
15	Data 4	Data bit 4	I
16	Data 3	Data bit 3	I
17	Data 2	Data bit 2	I
18	Data 1	Data bit 1	I
19	Data 0	Data bit 0	I
20	VDD	Supply Voltage 2.9V	N/A

## 13 Slider Open – Close Detection

The Hall-sensor is used in the EL71 to detect the position of slider.

The Hall-sensor is supplied from logic voltage 2.65V. The output is connected directly to SGOLD2. If a magnetic field is detected from the Hall-sensor the output line will switch to low signal and generate an interrupt.



## 14 EL71 Diagram Sets

Double click the tag symbol to open the files.



TD\_Repair\_EL71  
Diagram Set\_R1.0.pdf



TD\_Repair\_EL71\_Logic  
Diagram\_R1.0.pdf



TD\_Repair\_EL71\_RF  
\_HIT\_Diagram\_R1.0.